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Analysis and Design of Operational Transconductance Amplifier (OTA) using Cadence tool

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Abstract: **This paper represents the analysis and design of two-stage operational transconductance amplifier (OTA) used in switched-capacitor (SC) circuits. The existing design methods for two-stage OTAs often lead to sub optimal solutions because they decouple inter-related metrics like noise and settling performance. In this approach, the cadence tool is used to analysis the transient response, AC response and phase plot of the OTA and also the settling time has been observed on the simulation. For the optimization routine, there is no need to interface with a circuit simulator because all significant devices parasitic are included in the tool. The simulation results show that a 90-nm prototype amplifier achieves the settling time of 1.5 ns with reduced integrated noise while consuming 2.3 mW from a 1.1V power supply with phase plot for 174 degree.**

Keywords: **Two stage OTA, transient response, settling time, power, cadence tool.**

I. INTROUDUCTION

The recent rapid development in VLSI technology the size of CMOS devices decreases and power supply also decreases. The OTA is a basic building block in most of analogue circuit with linear input-output characteristics. The OTA is popular for implementing voltage controlled oscillators (VCO) and filters (VCF) for analog music synthesizers, neural networks and instrumentation amplifier because it can act as a two-quadrant multiplier [1]. Fast, high gain operational-transconductance-amplifiers (OTAs) are an integral part of switched-capacitor (SC) circuits [2]. The primary application for an OTA is however to drive low-impedance sinks such as coaxial cable with low distortion at high bandwidth. The OTA has been traditionally implemented using a cascade of two stages to provide a high gain. Scaling dimensions in CMOS technology requires proportional scaling in supply voltage as well. Though lower supply voltages result in lower power consumption, as the supply currents [3]. Improving the settling performance by Phase-margin adjustments has been proposed in the literature. However, for two-stage amplifiers, better phase margin does not always imply faster settling [4]. An OTA is a voltage controlled current source, more specifically the term “operational” comes from the fact that it takes the difference of two voltages as the input for the current conversion.

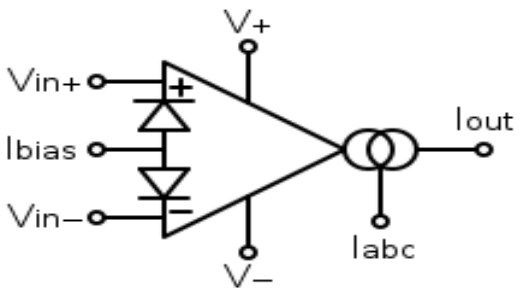

Fig.1 Ideal OTA

The ideal transfer characteristic is therefore

$I_{out} = g_m (V_{in}+ - V_{in}-)$ (1)

or, by taking the pre-computed difference as the input,

$I_{out} = g_m * V_{in}$ (2)

with the ideally constant transconductance g_m as the proportionality factor between the two. In reality the transconductance1 is also a function of the input differential voltage and dependent on temperature. To summarize, an ideal OTA has two voltage inputs with infinite impedance (i.e. there is no input current). The common mode input range is also infinite, while the differential signal between these two inputs is used to control an ideal current source (i.e. the output current does not depend on the output voltage) that functions as an output. The proportionality factor between output current and input differential voltage is called transconductance [5].

The paper is organized as follows. In Section II, we start by discussing why closed form symbolic expressions are important for analog design automation and optimization. In Section III, we describe the two-stage OTA specifications, schematic, and behavioural model. Conclusions are provided in Section VI.

II. ANALOG DESIGN AND OPTIMIZATION USING CADENCE TOOL

For larger circuits, symbolic analyzers and/or simulators can be used to perform the automated design and optimization. The gradients and Hessian matrices can be found by two methods. The optimization algorithm can perturb each variable and use the simulator to evaluate the objective and constraints and then compute the gradients and Hessians using finite differences (a slow process), or simply use the symbolic model to find the gradients directly by differentiation over the closed form expressions of the objective and constraints (a fast process).

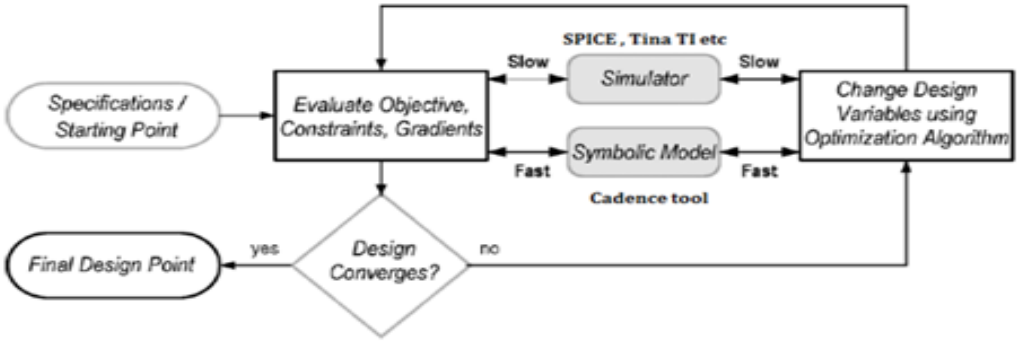

Fig.2. Analog design automation and optimization.

Sometimes, the optimizer can reach a design point that is feasible, but finite differences around lead to an infeasible point, causing the optimizer to diverge or halt prematurely. In such cases, providing gradients and Hessians directly from closed form expressions allows the optimizer to converge to a solution [6], [7].

A typical design optimization loop is shown in Fig. 2. The design starts with a certain set of specifications and a starting point. The performance metrics are evaluated at the current design point. This can be done by going back to the simulator, which is a very slow process. By using a complete symbolic model in cadence tool, which is faster than the previous. The optimization algorithm then changes the design point to make sure that the objective converges to the optimum and the constraints are met.

We thus conclude that finding the gradient using finite differences can be time consuming, can lead to inaccurate results, and may even cause the optimizer to fail. This can be especially problematic when the optimizer needs to be run multiple times with new starting points, in order to find the globally optimal design point. Each optimizer run itself involves multiple transient, noise, and ac simulations. This leads to impractically long run times if a circuit simulator is used, even for small and medium sized circuits. All these problems can be overcome if closed form symbolic expressions are available and are used for generating the gradients and Hessians. Such expressions speed up computer-based optimizations, and can sometimes provide designers with design in-sights and trade-offs, letting them make intelligent design choices. Designers can use closed form equations to analyze a circuit and prepare a fixed design plan that can be used for the knowledge-based approach to analog design automation [8].

III. TWO-STAGE OTA DESIGN AND OPTIMIZATION—MODEL DESCRIPTION

In this section, we describe the model used for the design and optimization two-stage OTA using cadence tool. The CMOS level implementation of the OTA is shown in Fig. 3.

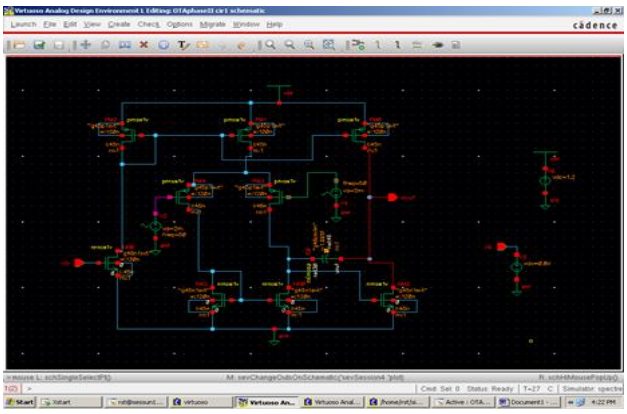

Fig. 3. Design of two stage OTA using cadence

We start with a list of specifications summarized in Table I. These assumed values are for a typical 3 stage OTA gain stage clocked at 1Hz to 125 MHz, which finds applications in pipelined ADCs and SC delta-sigma modulators. The dynamic error specification of 0.1 implies that the output should settle to within± 0.1% of the final steady state value within 1.6 ns (1/2 clock cycle) when the supply voltage is given as 1.2V.

CMOS M1: The lowest common-mode input voltage, V_{cm}; min imposes the toughest constraint on CMOS M1 remaining in saturation. CMOS M2: The systematic offset condition makes the drain voltage of M1 equal to the drain voltage of M2. Therefore, the condition for M2 being saturated is the same as the condition for M1 being saturated. Note that the minimum allowable value V_{cm}; min is determined by M1 and M2 entering the linear region. CMOS M3: Since V_{gd3}=0 CMOS M3 is always in saturation and no additional constraint is necessary. CMOS M4: The systematic offset condition also implies that the drain voltage of M4 is equal to the drain voltage of M3. Thus M4 will be saturated as well. CMOS M5: The highest common-mode input voltage, V_{cm}; max, imposes the tightest constraint on CMOS M5 being in saturation the maximum allowable value of V_{cm}; min is determined by M5 entering the linear region. CMOS M6: The most stringent condition occurs when the output voltage is at its minimum value V_{out}; min. CMOS M7: For M7, the most stringent condition occurs when the output voltage is at its maximum value V_{out}; max. CMOS M8: Since V_{gd8}=0, CMOS M8 is always in saturation [9].The amplfied output (V_{out}) on the final stage is shown in the Fig.4. The output voltage is lies between the 1.0725V and 1.0825V. So that the low power is consumed while apply frequency is 31.974KHz.The transient response and the phase shift on the different node is clearly shown on the netlist files respectively.

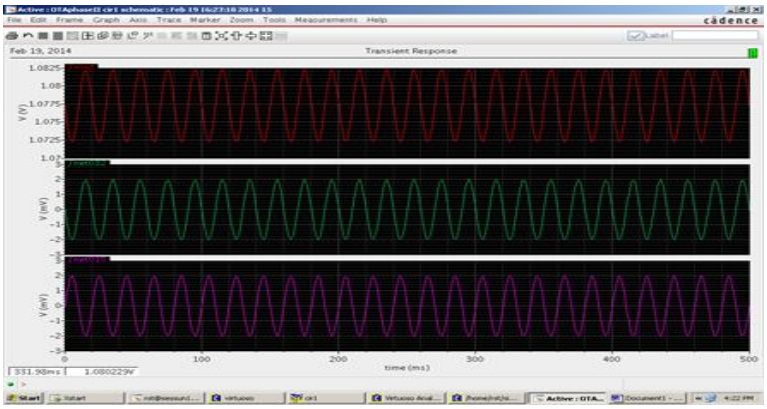

Fig.4. Amplified output on cadence tool

Since the AC frequency response is an important factor for any amplifier which helps to calculate the bandwidth and also the gain. The AC frequency response is remaining constant up to the 10MHz and the maximum voltage on the frequency response is about 5.03mV. By operating all CMOS in to saturation region, the power consumption and slew rate is reduced but gain Bandwidth product remains constant. The simulated output frequency response is shown in Fig.5. If the

OTA is designed on the 130nm and 180nm level the intrinsic gain has been increased 30 and nearby 50 respectively. In this approach the OTA is designed in the level of 90nm on cadence tool.

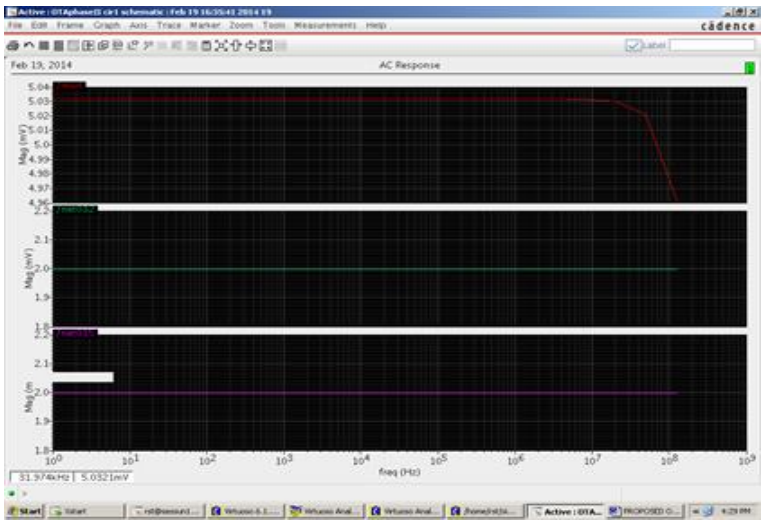

Fig.5. AC response of two stage OTA

The intrinsic gain of the CMOS used in these amplifiers has reduced dramatically due to technology scaling (g_m*r_0 >15 for 90-nm CMOS). The V_{DS} is reduced when the OTA is designed on the 90nm level is shown on the Fig.6. In addition, due to voltage headroom constraints, it has become increasingly difficult to use cascoding as a solution to this problem. Thus, as an alternative, it is attractive to consider cascades of more than two common-source stages to achieve high dc gain [10].

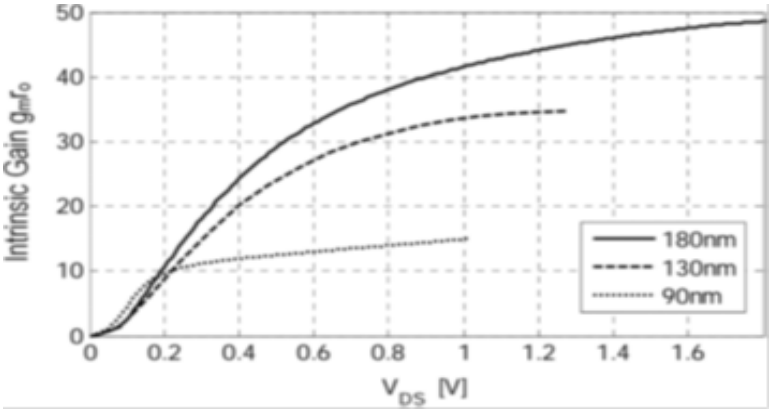

Fig.6. CMOS intrinsic gain on various size nm

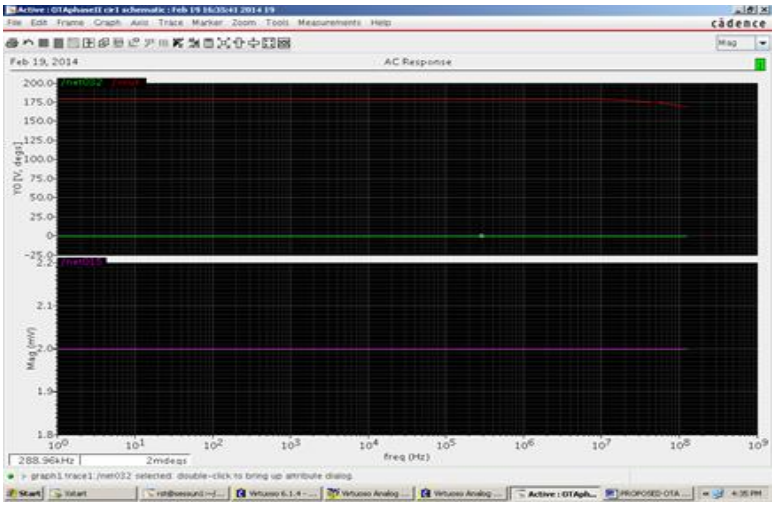

Fig.7. Phase plot AC response for 2 stage OTA

The AC response phase plot of the designed OTA is shows in the Fig.7 which deals with the degree of 175 while applying the input voltage as DC 2V. The phase can be decayed while it reaches the frequency is about the 10MHz.

IV. CONCLUSIONS

TABLE I. Comparison of Parameters

Parameters	Existing	Proposed (cadence)
Technology	350nm	90nm
Number of CMOS used	9	9
Settling time	<2.5ns	Around 1.6ns
Power	3.4mW	2.3mW
Gain	2	Gain plot constant up to 10MHz
Phase	-	Shows 175 deg

Design of OTA is vital importance in integrated Continuous-time filters. A 90nm two OTA with gain has the steady state response up to 10 MHz boosting technique and it consume less power consumption is about the 2.3mW. This OTA can further be used for analog portable devices. The behavioral simulation indicates that settling time is 1.5 ns for the GBW of 10MHz are sufficient to design modular circuit of Digital-Audio Sigma-Delta modulator. As we have shown this leads to a fast optimization program, while maintaining close matching to circuit-level simulation.

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