SURVEY ON 1-BIT FULL ADDER DESIGN IN QUANTUM DOT CELLULAR AUTOMATA

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Abstract: Quantum-dot cellular automata are one of the best alternative technologies of CMOS at nano-scale. It is an emerging technology promising to design circuits with low power consumption, high density as well as high speed. Nanotechnology based QCA basic logic layouts work well while simulating on QCA Designer software. The full adder circuit is a basic unit in digital arithmetic and logic circuits. The design of adders has been reported by various researchers and most of the circuit combinations produce excellent results on simulation. We will understand in this paper to different type of full adder design and formulation to design it. We also try to design QCA full adder design using a different formula for sum and carry which is enhanced in term of cell numbers in comparison to other approaches Although design of QCA full adders has been reported by a large number of researchers but the simulation results on most of the circuits fail to produce claimed outputs as such the carry forward work is becoming difficult. There are certain difficulties in producing desired simulation results while joining two half adders to design full adder. The main cause for the problem seems to be the mismatch of input data, when earlier stage data is combined with the forward stage.

We are study and try to design our own circuitry to overcome issue on complex relation for designing a full adder with two half adder policy rather than we try to separate structure for full adder circuitry to improvise the desired result and minimum requirement of quantum cells. For This purpose we allow to choose different methodology and design techniques. We have tried to study some full adder designs on the basis of simulation results to move forward with our own designs for the purpose.

Keywords: Quantum Dot Cellular Automata, Nano Technology' QCA full adder, QCADesigner.

I.   INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) has anticipated that size point of confinement of CMOS innovation will be constrained to around 5 nm to 10 nm and trusts this cutoff will be come to as ahead of schedule as 2017 [3]. The cutting edge processing devices are quantum PCs which depend on quantum mechanics. Quantum PCs depend on energy of photon and electron properties for performing figuring handling. They are parallel preparing that is a great many operations at any given moment. So the preparing velocity of a 30 q-bit quantum PC will be in the scope of TeraHertz (THz). The latest advances that is being examined. The circuits engaged with quantum based PCs can be produced from the quantum dot gates and circuits-

John von Neumann, a Hungarian mathematician presented the idea of cell automata. The possibility of quantum calculation is by and large included to Feynman who proposed a computational model in view of quantum mechanical laws. The discrete idea of cell mechanization and quantum mechanics prompts the development of nanoscale circuits to perform calculation. One conceivable approach to keep up the development in circuit density is to change from CMOS based worldview to nanoscale extends. The primary favorable circumstances of such circuits high speed, high design density, little measure of energy utilization and there by energy saving. A quantum dot cell automata (QCA) is a rising nanotechnology.

In QCA, a cell binds two free electron and the logic values '0', '1'depends on position of electrons inside the quantum-dot cell, which are driven by Coulombic interaction. Different QCA based digital circuits have been investigated in recent years; structures for 5-input majority gate [5-13], designs for a one bit full adder [6, 9, 11, 52], QCA based memory cells, flip flops have also been studied. In most of the work, designs are not robust and vulnerable to fabrication defects due to wire crossing between the QCA components. So, an efficiently design of crossover wires can reduce the overall costs (i.e., both cell count and implementation complexity). Multilayer crossing is not favorable, due to its area overhead and fabrication issues [17]. However, coplanar crossover is achieved by the use of 450 rotated QCA cells [16], but end up with problems, such as reduce robustness and high implementation cost [17], due to two types of QCA cells. The idea behind this work is to devise area efficient and robust QCA circuits using single type cell, and analyze the power dissipation of existing and proposed majority gates. The proposed full adder design requires a lesser number of cells and draws little power compared to the best reported one in literatures. Further, an optimal single layer one bit full adder is designed by considering majority gate, which is based on single type cell.

II.   TECHNICAL BACKGROUND

Quantum-Dot Cellular Automata (QCA) is another nano technology worldview which encodes twofold data by charge setup inside a phone rather than the regular current switches. There is no present stream inside the cells since the columbic cooperation between the electrons is adequate for calculation. This worldview gives one of numerous conceivable answers for transistor-less calculation at the nanoscale. The standard QCA cells have four quantum dots and two electrons [16]. There are different dots of QCA cells proposed which incorporate a six-dot QCA cell and an eight-dot QCA cell. In a QCA Cell, two electrons possess askew inverse spots in the cell because of shared shock of like charges. A case of a basic unpolarized QCA cell comprising of four quantum dots masterminded in a square is as appeared in Fig.1 dots are basically puts where a charge can be limited. There are two additional electrons in the cell those are allowed to move between the four dots. Burrowing in or out of a cell is smothered. The numbering of the dots in the cell goes clockwise starting from the dot on the top right.
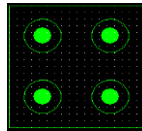

Figure: - 1 Simple 4-dot Unpolarized QCA cell.

A polarization P in a cell, that measures the extent to which the electronic charge is distributed among the four dots, is therefore defined as:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4}$$

Where **ρi** is the electronic charge in each dot of a four dot QCA cell. Once polarized, a QCA cell can be in any one of the two possible states depending on the polarization of charges in the cell. Because of columbic repulsion, the two most likely polarization states of QCA can be denoted as P = +1 and P = -1 as shown in Fig.2. The two states depicted here are called most likely and not the only two polarization states because of the small (almost negligible) likelihood of existence of an erroneous state.
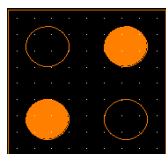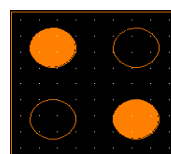

Figure:-2 P = +1 Binary Logic1   **P = - 1 Binary Logic 0**

LOGICAL DEVICES IN QCA

As found in the past areas, the data in QCA cells is exchanged due to columbic cooperation's between the neighboring QCA cells; the condition of one cell impacts the condition of the other.

Binary Wire

A paired wire can be seen as an even arrangement of cells to transmit data starting with one cell then onto the next. A case of a QCA wire is as appeared in Fig. 3. A parallel wire is regularly separated into different clock zones, to guarantee that the flag doesn't fall apart as signs for the most part have a tendency to debase with a long chain of cells in a similar timing zone.
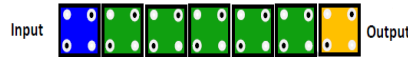

Figure: - 3 A QCA binary wire Realization

Inverter

Two diagonally aligned cells will have the opposite polarization. Henceforth, inverters can be implemented with lines of diagonally aligned cells. An example of a QCA Inverter is as shown in Figure
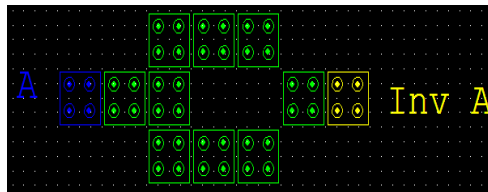

Figure: - 4 QCA designed inverter circuits

Majority Gate

Majority Gate (MV) is the fundamental logic block in any QCA design. A majority gate can be built with the help of five cells. The top, left and bottom cells are inputs. The device cell in the centre interacts with the three inputs and its result (the majority of the input bits) will be propagated to the cell on the right. An example of an MV representation in QCA is as shown in Figure 5. The logic function implemented by the MV is

$$f(A, B, C) = A.B + B.C + C.A$$

Consider the Coulombic cooperation between cells 1 and 4, cells 2 and 4, and cells 3 and 4. Coulombic connection between electrons in cells 1 and 4 would typically bring about cell 4 changing its polarization in light of electron aversion (accepting cell 1 is an info cell). Notwithstanding, cells 2 and 3 additionally impact the polarization of cell 4 and have polarization P=+1. Therefore, on the grounds that most of the cells impacting the gadget cell have polarization P=+1, it too will likewise accept this polarization on the grounds that the powers of Columbic collaboration are more grounded for it than for P=-1.
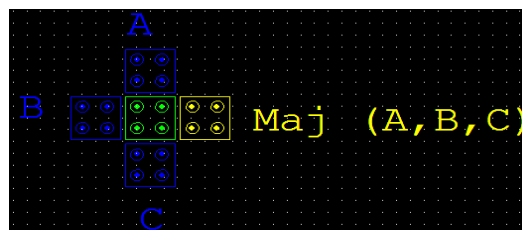

Figure:-5 A three input majority gate

THE QCA CLOCK

This section will clarify and talk about how the QCA clockworks. Not at all like the standard CMOS clock, has the QCA clock had more than a high and a low stage. The periods of the QCA clock and illustrations are talked about underneath.

The check in QCA is multi-staged. Individual QCA cells are not planned independently. The wiring required to clock every phone exclusively could without much of a stretch overpower the disentanglement won by the natural neighborhoods interconnectivity of the QCA design [8]. Four phase switching realized in each clocking phase for different clock zones. Information flows in a pipelined fashion from inputs towards outputs during four clock zones.
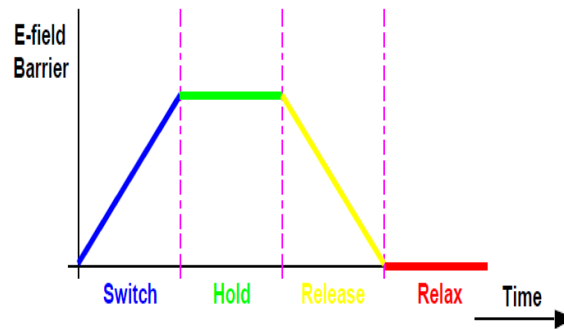
Figure: - 6 the four phases of the QCA clock

Now and time it merits specifying that there is some characteristic pipelining incorporated with the QCA innovation. After each 4 time steps, it is conceivable to put another esteem onto a QCA wire.

CROSSING

In QCA structures fabrication of interconnection between components needs to be handled efficiently for a better stability. Till now, there are two different types of crossover are available. These are coplanar and multilayer. In multilayer crossover, multiple layers are used as in CMOS circuit design for interconnection between components. In coplanar crossover strategy, wire crossing is done by two different cells. These cells are orthogonal to each other, so they operate without affecting neighboring cells. The first wire consists of cells of 90^0 orientations and second wire has only 45^0 orientations as shown in Figure 8. The main drawback of this scheme is that any misalignment of cells during fabrication may cause a cross coupling between the two wires. Works have been done to mitigate such effects, and also to increase the robustness of the circuits, but all these end up with large area overhead [14, 19].
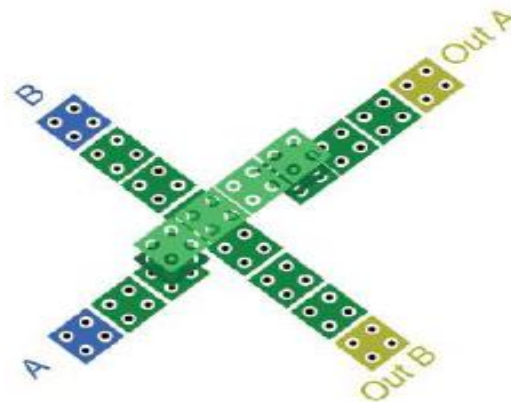

Figure: - 7 Crossover diagram different orientation

III.   PROBLEM IDENTIFICATION

In late year, numerous Researchers have proposed too many 1-bit full adder compositional designs in Quantum Dot Cellular Automata neno-technology applications by various procedures like traditional, when legitimately planned; can be over twice as quick as static rationale. It utilizes just the quicker Q-cell, which enhance region of rationale advancements. Static logic is slower on the grounds that it has double the capacitive stacking, higher limits, and uses dormant q-bits for logic circuits. Rationale can be harder to work with, however it might be the main decision when expanded handling speed is required. In regular CMOS rationale style, this rule can be rethought as an announcement that there is dependably a low-impedance DC way between the yield and either the supply voltage or the ground

In 1-bit full adder plans the spread deferral and vitality utilization of the Quantum Dot Cellular Automata are most basic issue when we enhance the delay than a similar time control utilization increments. Tradeoff between energy consumption and propagation delay by different– different methodology work on the parameter of neno-technology. With this new methodology we improve both of them simultaneously without decreasing the basic characteristics of the circuit

DRAWBACKS

- The power dissipation in this circuit is more than the previous circuits. However with same power consumption it performs faster.

- But the use of substantial number of external fixed input results in high energy utilization, more power consumption and larger area.

- The major problem of revisable designs is that it requires more area and quantum bit to process to realize. Thus, it will be more expensive to realize QCA circuits. Moreover if only standard logic gate we need in the circuit than that are not feasible for our design.

- The power dissipation in this circuit is more than the exiting full adder circuits. However with less effective area, higher fan-out and same power consumption it performs faster.

But the use of substantial number of quantum cell in low input loads, more power consumption and small silicon area

IV. RELATED WORKS

Various QCA full-adders have been presented to date. The first one (presented in 1994) is composed of five three-input majority gates and three inverters (Tougaw and Lent, 1994). This full-adder uses QCA coplanar wire.

Hashemi et al. 181 crossing scheme. It is implemented in one layer using 192 QCA cells. In this design QCA clocking concepts are not considered. In Vetteth et al. (2002) another QCA full-adder using the same logical structure and coplanar wire crossing scheme is presented. In contrast to the previous design, this full-adder incorporates QCA clocking scheme and takes 14 clock phases (3.5 clock cycles) to generate outputs. This full-adder was used in designing a 4-bit CLA (Vetteth et al., 2002). A simpler QCA full-adder is presented in (Wang et al., 2003). This full-adder is composed of three three-input majority gates and two inverters (Wang et al., 2003). It uses QCA coplanar wire crossing scheme and takes 5 clock phases (1.25 clock cycles) to produce outputs. Hence, it is faster than presented design in (Vetteth et al., 2002). The schematic of this full-adder is shown in Figure 10. Different layouts for this schematic have been presented to date (Cho and Swartzlander, 2007, 2009; Cho, 2006; Hänninen and Takala, 2010; Kim et al., 2007; Zhang et al., 2005). The presented QCA full-adder in (Zhang et al., 2005) utilizes QCA multilayer wire crossing scheme and is simpler than previous design (Wang et al., 2003) in terms of cell count. It produces outputs in 4 clock phases (1 clock cycles); hence, it is faster than the previous designs. In the study of Cho and Swartzlander (2007) another QCA full-adder using the same logical structure and multilayer wire crossing scheme is presented. It takes 5 clock phases (1.25 clock cycles) to produce outputs. This full-adder was used to implement three kinds of adders (Ripple carry adder, carry look ahead adder and conditional sum adder) with large word sizes (Cho and Swartzlander, 2007). These adders were compared in terms of area, complexity (cell count) and delay (Cho and Swartzlander, 2007). Two other QCA full-adders (presented as Type I and II) using five gates (three majority gates and two inverters) are introduced in (Cho, 2006). These designs utilize QCA multilayer wire crossing scheme. The presented adder as Type II is more efficient in designing large adder circuits (Cho and Swartzlander, 2009; Cho, 2006). It is constructed using 86 QCA cells and takes only 3 clock phases (0.75 clock cycles) to produce outputs. This full-adder dominates all the previous designs in terms of area, complexity (cell count) and delay. In Hänninen and Takala (2010); Kim et al. (2007) robust QCA full-adders are presented. These designs use the coplanar wire crossing scheme for crossover wires. The presented design in (Hänninen and Takala, 2010) surpasses the presented design in (Kim et al., 2007) in terms of area, delay and complexity (cell count). Another QCA full-adder design is presented in (Rahimi et al., 2007). This adder is constructed using unconventional form of QCA cells. It is composed of two majority gates and one inverter. In this design in contrast to the previous structures, implemented using three-input majority gates, one of the majority gates is a five-input voter. In order to implement this schematic, a cubic design for QCA cells is presented in (Rahimi et al., 2007). This cubic cell has six sides and can be used to implement a five-input majority gate (Rahimi et al., 2007).

Finally the last one design based A novel 3-input XOR gate based on the cellular interaction is first proposed which consists of 10 cells and requires two clocks. To demonstrate the efficiency of the proposed XOR gate, an optimized single layer full-adder is designed here which contains only 20 cells and requires three clock phases.

Table 1:- The list of previous single-layer full-adder

Designs	MVs	NOTs	Cells	Clock phases
R.Zhang et al., 2005 [52]	3	2	93	4
H.Cho, 2006 [53]	3	2	82	3
H.Cho et al., 2007 [54]	3	2	135	5
H.Cho, 2009 [55]	3	2	73	3
K.Navi et al., 2010 [18]	2	2	73	3
K.Navi et al., 2010 [56]	2	2	61	3
B.Bishnoi et al., 2012 [57]	2	2	95	8
S.Hashemi et al., 2012 [58]	2	2	51	3
V.Pudi and K.Sridhara, 2012 [59]	3	1	79	4
S.Hashemi et al., 2012 [58]	2	2	79	5
A. Roohi et al., 2014 [60]	2	2	52	3
S.Sayedsalehi et al., 2015 [27]	3	2	105	3
A. Roohi et al., 2015 [15]	2	2	23	3
M. Mohammadi et al., 2016 [13]	3	2	38	3
A. Safavi and M.Mosleh, 2016 [51]	2	3	31	3
S.Seyedi and N.J.Navimipour, 2017 [8]	2	2	22	3

Table 2:- List of previous multi-layer full-adders.

Designs	MVs	NOTs	Cells	Clock phases
C.Lent et al., 1994 [5]	5	3	192	NA
W. Wang et al., 2003 [4]	3	2	105	4
Zheng et al., 2004 [47]	3	2	145	4
K. Kim et al., 2007 [48]	3	2	220	12
L. Hanninen et al., 2010 [49]	3	2	102	8
M. Rahimi et al., 2012 [50]	2	1	>107*2	NA
S.Angizi et al., 2014 [39]	2	2	95	5
S. Hashemi and K. Navi, 2015 [44]	2	3	71	6
D.Abedi et al., 2015 [17]	3	2	59	4
T.Sasamal et al., 2016 [12]	2	2	49	4
S.R.Heikalabad et al., 2017 [10]	5	1	41	4
H. Rashidi and A. Rezai, 2017 [9]	3	2	33	2
M.Balali et al., 2017 [11]	2	2	29	2

V. QCADESIGNER TOOL

Initially developed at the ATIPS Laboratory, University of Calgary, QCADesigner has attracted some important new developers, including top researchers from the University of Notre Dame. The project is written in C/C++ and employs a wide range of open-source software such as the GTK graphics library, and is maintained under the GNU public license for open source software. Developing the project in this manner enables it to be compiled and used on a wide range of systems. The objective of the project is to create an easy to use simulation and layout tool available freely to the research community via the Internet. One of the most important design specifications is that other developers should be able to easily integrate their own utilities into QCADesigner. This is accomplished by providing a standardized method of representing information within the software. As well, simulation engines can easily be integrated into QCADesigner using a standardized calling scheme and data types.

Programming bundles that plan, format, and help in the manufacture of incorporated circuits have disentangled the outline procedure and lessened an opportunity to-advertise for some circuits. Specifically, planning a circuit once for all creation advancements, rather than another outline for each assembling innovation, incredibly extended the extension and capacity of these outline devices. This detachment amongst engineering and innovation was effectively actualized by means of the

Caltech Interchange Format or CIF [15]. Current QCA configuration devices have not yet built up a document arrange that backings the partition amongst engineering and innovation. Also, each plan device keeps on utilizing its own document arranges. Hence, a QCA circuit architect can't plan and reenact a similar circuit with different apparatuses without updating it each time.

Both of these restrictions have been removed in this thesis by developing a set of file formats for QCA circuit design. There are two formats dedicated to detailing the circuit architecture with no technology-dependent information contained in them. A third format has been created that contains the specific technology information used to implement a QCA circuit. These formats are based on the XML (eXtensible Markup Language) standard, thus, any design tool could be capable of using these file formats.

VI.   CONCLUSION

This report contain the most of the part of the full adder deigning practices in Quantum cellular automata with different methodologies that make simple design via comparing with that previous one. But most of them design with using two half adder method and some of other who try separate design they use multi layer design.

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