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SURVEY ON MULTIPLEXER DESIGN USING QUANTUM DOT CELLULAR AUTOMATA

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Abstract: **The quantum-dot cellular automata (QCA) technology is a promising alternative technology to CMOS technology to extend the exponential Moore's law progress of microelectronics at nanoscale level, which is expected to be beneficial for digital circuits. Quantum dot Cellular Automata are future representations of quantum reckoning, which is developed in resemblance to the predictable models of cellular automata familiarized by Von Neumann. Multiplexer is an important building block of digital circuits and very useful part in most frequently used logical circuits. The previous study of multiplexer designs simulates the basic elements or Combinational circuit. The results demonstrate that the previous QCA multiplexer architectures have the best performance in terms of clock delay, circuit complexity, and area in comparison with older QCA multiplexer architectures, day by day improvement reflected in the reechoes there is very tuff to analysis for new approaches to design new multiplexer circuits before we find few drawback in previous design and now we study most of the fine multiplexer design here. A 2:1 multiplexer has been designed and implemented before with the help of majority voters and successfully implemented in QCA. The MUX is more robust and enjoys single layer and single clock wire crossing, which requires only one type of cell .we try to design multiplexer circuit performs equally well compared to existing designs.**

We are study and try to design our own circuitry to overcome issue for this purpose we allow to choose different methodology and design techniques. QCADesigner software is used to create a detailed layout and for circuit simulation. The circuits simulated using QCADesigner.

Keywords: **Quantum Dot Cellular Automata, Nanotechnology, Multiplexer, QCADesigner-2.0.3.**

I. INTRODUCTION

Due to the dramatic increase rate in the number of transistors within the chip, reducing the size of transistors is essential, however in the CMOS technology, size reduction of transistors, at nano-scale, isn't always possible actually and the extension of Moore's regulation in CMOS era past 10-nm isn't always possible as it introduces an anomalous quantum conduct in nanoscale .The quantum-dot cellular automata (QCA) technology is able to achieve higher speed and density and lower power consumption designs compared to conventional CMOS technology. The binary information in this technology is encoded by reconfiguration of the charges instead of current. So in recent years, circuit implementation in QCA technology has received a great deal of attention due to a number of promising applications such as efficient QCA full adder design [6–9], efficient QCA multiplier design [10,11], and efficient QCA multiplexer design.

A John von Neumann, a Hungarian mathematician presented the idea of cell automata. The possibility of quantum calculation is by and large included to Feynman who proposed a computational model in view of quantum mechanical laws. The discrete idea of cell mechanization and quantum mechanics prompts the development of nanoscale circuits to perform calculation. One conceivable approach to keep up the development in circuit density is to change from CMOS based worldview to nanoscale extends. The primary favorable circumstances of such circuits high speed, high design

density, little measure of energy utilization and there by energy saving. A quantum dot cell automata (QCA) is a rising nanotechnology.

QCA is a new digital system for next generation [3–4]. Majority gate [4] and Inverter cell [4] are two main primitive logic gates for circuit designs in QCA nanotechnology. Till now various QCA based logic.

Circuits have been implemented [4–15]. Majority gate [4] and Inverter cell [4] has desirable features to implement logic for QCA. However, still the logic is not competent and research is continuous due to the current trends of complexity, power and area constraints. Majority gate & Inverter cannot reduce the circuit complexity and maximizes the device density in QCA circuits alone. These gates are not functionally complete to design all logic circuits. The main focus of all new techniques is to reduce circuit parameters and excels these major issues. Multiplexer is the most frequent combinational component used in digital logic systems. The multiplexer is a very useful electronic circuit that has uses in many different applications such as signal routing, data communications and data bus control applications. Based on this various arrangements of the QCA cells widespread range of QCA multiplexers designs are realizable [5–15].

Efficient QCA Multiplexer (MUX) design is a problem that has been brought the attention of the research community. Many research works have been carried out to design an efficient multiplexer [5–15]. Multiplexer are used in various fields where multiple data need to be transmitted using a single line.

RESERCH OBJECTIVES

- To build up an approach/philosophy which decreases control utilization and propagation delay adequately when contrasted with approaches/technique that have been proposed in past for multiplexer design outline.
- To improve the Logical operation with less area multiplexer design circuit with powerfully change plan for various Boolean capacity as indicated by their execution in the circuit. So we can enhance the come about without utilizing additional natural.
- Design and recreation of proposed multiplexer quantum cell structures with diminished settled information techniques to tradeoff between power, Area and speed of outlines.

II. TECHNICAL AND BACKGROUND

- Quantum-Dot Cellular Automata (QCA) is another nano technology worldview which encodes twofold data by charge setup inside a phone rather than the regular current switches. There is no present stream inside the cells since the columbic cooperation between the electrons is adequate for calculation. This worldview gives one of numerous conceivable answers for transistor-less calculation at the nanoscale. The standard QCA cells have four quantum dots and two electrons [16]. There are different dots of QCA cells proposed which incorporate a six-dot QCA cell and an eight-dot QCA cell. In a QCA Cell, two electrons possess askew inverse spots in the cell because of shared shock of like charges. A case of a basic unpolarized QCA cell comprising of four quantum dots masterminded in a square is as appeared in Fig.1 dots are basically puts where a charge can be limited. There are two additional electrons in the cell those are allowed to move between the four dots. Burrowing in or out of a cell is smothered. The numbering of the dots in the cell goes clockwise starting from the dot on the top right.

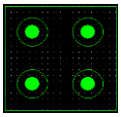

Figure: - 1 Simple 4-dot Unpolarized QCA cell.

A polarization P in a cell, that measures the extent to which the electronic charge is distributed among the four dots, is therefore defined as:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4}$$

Where ρi is the electronic charge in each dot of a four dot QCA cell. Once polarized, a QCA cell can be in any one of the two possible states depending on the polarization of charges in the cell. Because of columbic repulsion, the two most

likely polarization states of QCA can be denoted as P = +1 and P = -1 as shown in Fig.2. The two states depicted here are called most likely and not the only two polarization states because of the small (almost negligible) likelihood of existence of an erroneous state.

Figure:-2 P = +1 Binary Logic1 P = - 1 Binary Logic 0

LOGICAL DEVICES IN QCA

As found in the past areas, the data in QCA cells is exchanged due to columbic cooperation's between the neighboring QCA cells; the condition of one cell impacts the condition of the other.

Binary Wire

A paired wire can be seen as an even arrangement of cells to transmit data starting with one cell then onto the next. A case of a QCA wire is as appeared in Fig. 3. A parallel wire is regularly separated into different clock zones, to guarantee that the flag doesn't fall apart as signs for the most part have a tendency to debase with a long chain of cells in a similar timing zone.

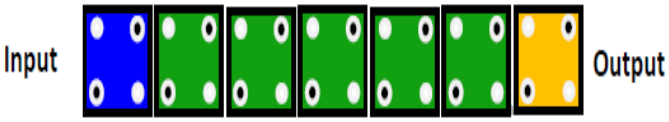

Figure: - 3 A QCA binary wire Realization

Inverter

Two diagonally aligned cells will have the opposite polarization. Henceforth, inverters can be implemented with lines of diagonally aligned cells. An example of a QCA Inverter is as shown in Figure.

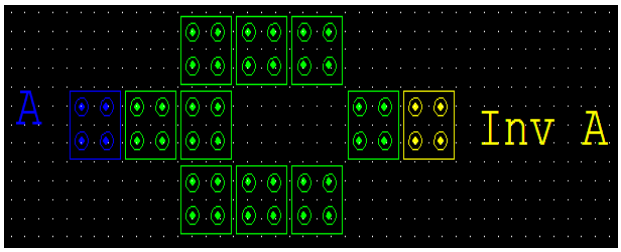

Figure: - 4 QCA designed inverter circuits

Majority Gate

Majority Gate (MV) is the fundamental logic block in any QCA design. A majority gate can be built with the help of five cells. The top, left and bottom cells are inputs. The device cell in the centre interacts with the three inputs and its result (the majority of the input bits) will be propagated to the cell on the right. An example of an MV representation in QCA is as shown in Figure 5. The logic function implemented by the MV is

$$f(A, B, C) = A.B + B.C + C.A$$

Consider the Coulombic cooperation between cells 1 and 4, cells 2 and 4, and cells 3 and 4. Coulombic connection between electrons in cells 1 and 4 would typically bring about cell 4 changing its polarization in light of electron aversion (accepting cell 1 is an info cell). Notwithstanding, cells 2 and 3 additionally impact the polarization of cell 4 and have polarization P=+1. Therefore, on the grounds that most of the cells impacting the gadget cell have polarization P=+1, it

too will likewise accept this polarization on the grounds that the powers of Columbic collaboration are more grounded for it than for P=-1.

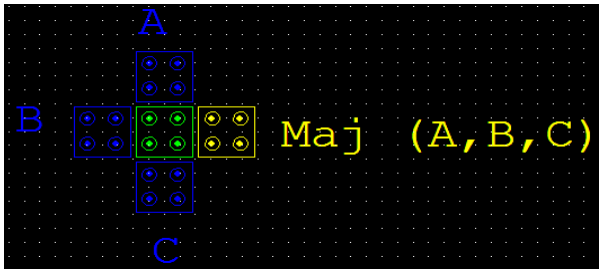

Figure:-5 A three input majority gate

THE QCA CLOCK

This section will clarify and talk about how the QCA clockworks. Not at all like the standard CMOS clock, has the QCA clock had more than a high and a low stage. The periods of the QCA clock and illustrations are talked about underneath.

The check in QCA is multi-staged. Individual QCA cells are not planned independently. The wiring required to clock every phone exclusively could without much of a stretch overpower the disentanglement won by the natural neighborhoods interconnectivity of the QCA design [8]. Four phase switching realized in each clocking phase for different clock zones. Information flows in a pipelined fashion from inputs towards outputs during four clock zones.

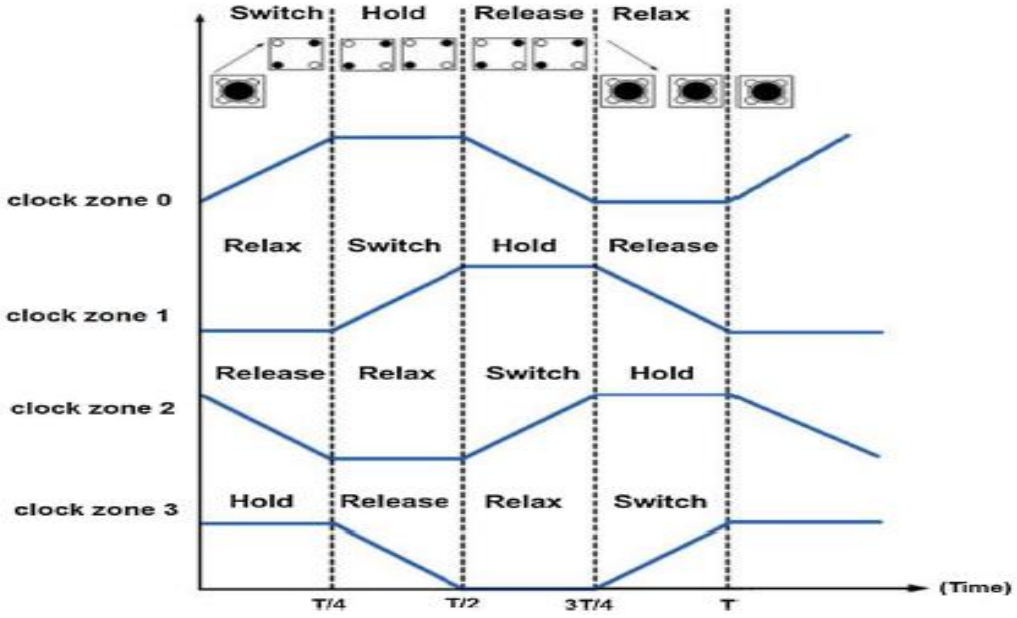

Figure: - 6 the four phases of the QCA clock

Now and time it merits specifying that there is some characteristic pipelining incorporated with the QCA innovation. After each 4 time steps, it is conceivable to put another esteem onto a QCA wire.

CROSSING

In QCA structures fabrication of interconnection between components needs to be handled efficiently for a better stability. Till now, there are two different types of crossover are available. These are coplanar and multilayer. In multilayer crossover, multiple layers are used as in CMOS circuit design for interconnection between components. In coplanar crossover strategy, wire crossing is done by two different cells. These cells are orthogonal to each other, so they operate without affecting neighboring cells. The first wire consists of cells of 900 orientations and second wire has only 450 orientations as shown in Figure 8. The main drawback of this scheme is that any misalignment of cells during fabrication may cause a cross coupling between the two wires. Works have been done to mitigate such effects, and also to increase the robustness of the circuits, but all these end up with large area overhead [14, 19].

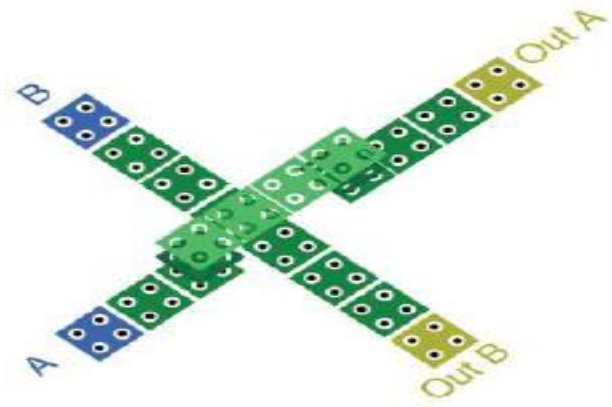

Figure: - 7 Crossover diagram different orientation

III. PROBLEM IDENTIFICATION

In In late year, numerous Researchers have proposed to Logic Gates compositional outline in Quantum Dot Cellular Automata neon-innovation applications by various procedures like traditional, when legitimately planned, can be over twice as quick as static rationale. It utilizes just the quicker Q-cell, which enhance region of rationale advancements. Static logic is slower on the grounds that it has double the capacitive stacking, higher limits, and uses dormant qubits for logic circuits. Rationale can be harder to work with, however it might be the main decision when expanded handling speed is required. In regular CMOS rationale style, this rule can be rethought as an announcement that there is dependably a low-impedance DC way between the yield and either the supply voltage or the ground

In Logic Gate plans the spread deferral and vitality utilization of the Quantum Dot Cellular Automata are most basic issue when we enhance the delay than a similar time control utilization increments. Tradeoff between energy consumption and propagation delay by different– different methodology work on the parameter of neon-technology. With this new methodology we improve both of them simultaneously without decreasing the basic characteristics of the circuit

DRAWBACKS

- The power dissipation in this circuit is more than the traditional digital gates. However with same power consumption it performs faster.
- But the use of substantial number of external fixed input results in high energy utilization, more power consumption and larger area.
- The major problem of revisable gates is that it requires more area and quantum bit to process to realize. Thus, it will be more expensive to realize basic digital gates. Moreover if only standard logic gate we need in the circuit than that are not feasible for our design.
- The power dissipation in this circuit is more than the traditional digital gates. However with less effective area, higher fan-out and same power consumption it performs faster.
- But the use of substantial number of quantum cell in low input loads, more power consumption and small silicon area.

IV. RELATED WORKS

Based on various arrangements of the QCA cells widespread range of QCA multiplexer designs have been reported in [5–15]. Kim et al. have analyzed the causes of the failure of QCA circuits and have proposed an adder circuit which utilizes a multiplexer with proper clocking scheme [5]. Multiple input QCA design depends on all the inputs which result in a variety of sneak noise paths in QCA [5]. They systematically analyzed the sneak noise paths in QCA- based design by using the concept of kink energy. And this analysis is significant due to its influence as the design size grows. They have also analyzed the failure of majority gates, and then they used the coplanar clocking technique in the design of full adder to overcome the errors. The multiplexer which has been used by them uses clock gating which is faster and smaller. Mardirisi and Karafyllid [6] have proposed modular 2n: 1 multiplexer which is formulated to increase the circuit stability. They have used the concept of crossover design for signal propagation and have shown each logic gate with blocks. Each block consists of two pairs of cells serially connected which produces signal delay equal to the number of included cell

pairs. Hashemi et al. [25] have proposed multiplexer in three layers in which the first layer is the backbone of the circuit. This new design is denser with four clocks latency and faster. In [10] Roohi et al. have designed 2:1 multiplexer using three clock zones due to this delay have been increased. In [10] Sen et al. have proposed a modular design of 2:1 MUX, with less delay involved.

QCA (Quantum-dot Cellular Automata) is an alternative technology for CMOS that has a low power consumption and high density. QCA extensively supports the new plans in the field of nanotechnology. Applications of QCA technology as an alternative method for CMOS technology in nano-scale have a hopeful future. Researchers successfully design implementation and simulation of 2-to-1, 4-to-1 and 8-to-1 multiplexer with the minimum area as compared to the previous models in QCA technology. The structure of the successful 2-to-1, 4-to-1 and 8-to-1 multiplexers, simulated in QCADesigner is provided. The multiplexers the minimum complexity, area and delay compared to the previous models. The implementation of 4-to-1 multiplexers is presented in QCA technique which has the minimum complexity and delay and 2-to-1 multiplexer is investigated from the cell missing and possible defects.

Quantum Cellular Automata (QCA) is an emerging nanotechnology and one of the top six technologies of the future. QCA are a transistor less computation approach which encodes binary information via configuration of charges among quantum dots.

The fundamental QCA logic primitives are majority and inverter gates which can be utilized to design various QCA circuits. Study presents a novel approach to designing efficient QCA-based circuits based on Boolean expressions achieved from reconfiguration of five-input and three-input majority gates. Whereas the multiplexer and Exclusive-or are the most important fundamental logical circuits in digital systems, designing efficient and single layer structures without coplanar cross-over wiring is advantageous in QCA technology. In order to demonstrate the efficiency and usefulness of the approaches, simple and dense multiplexer and Exclusive-or structures are implemented. The designs have significant improvement in terms of area, complexity, latency, and gate count in comparison to previous designs

Table 1:- The list of previous single-layer 2-to-4 decoder

DESIGN	AREA (nm)	CELL COUNT	Cell area (sq. nm)	EXTERNAL FIXED INPUT	NO OF CLOCK USED
Existing MUX 1	18144	23	7452	4	4
Existing MUX 2 [26]	21804	23	7452	2	3
Existing MUX 3 [21]	13924	17	5508	3	3

V. QCADESIGNER TOOL

Initially developed at the ATIPS Laboratory, University of Calgary, QCADesigner has attracted some important new developers, including top researchers from the University of Notre Dame. The project is written in C/C++ and employs a wide range of open-source software such as the GTK graphics library, and is maintained under the GNU public license for open source software. Developing the project in this manner enables it to be compiled and used on a wide range of systems. The objective of the project is to create an easy to use simulation and layout tool available freely to the research community via the Internet. One of the most important design specifications is that other developers should be able to easily integrate their own utilities into QCADesigner. This is accomplished by providing a standardized method of representing information within the software. As well, simulation engines can easily be integrated into QCADesigner using a standardized calling scheme and data types.

Programming bundles that plan, format, and help in the manufacture of incorporated circuits have disentangled the outline procedure and lessened an opportunity to-advertise for some circuits. Specifically, planning a circuit once for all creation advancements, rather than another outline for each assembling innovation, incredibly extended the extension and capacity of these outline devices. This detachment amongst engineering and innovation was effectively actualized by means of the Caltech Interchange Format or CIF [15]. Current QCA configuration devices have not yet built up a document arrange that backings the partition amongst engineering and innovation. Also, each plan device keeps on utilizing its own document arranges. Hence, a QCA circuit architect can't plan and reenact a similar circuit with different apparatuses without updating it each time.

Both of these restrictions have been removed in this thesis by developing a set of file formats for QCA circuit design. There are two formats dedicated to detailing the circuit architecture with no technology-dependent information contained in them. A third format has been created that contains the specific technology information used to implement a QCA circuit. These formats are based on the XML (eXtensible Markup Language) standard, thus, any design tool could be capable of using these file formats.

VI. CONCLUSION

We try to design an Efficient multiplexer with physical proof. To support this, a detailed analysis of structural and power issues of all prior ones. To investigate area, fixed external inputs and clock used using QCADesigner 2.0.3 tool. To showcase the efficacy in new designs, a new multiplexer structure was introduced, which inculcates coplanar non-crossover wires, via clock phasing. It is observed that these coplanar structures are robust for considerable variation in temperature and yield more compact digital circuits with respect to existing designs. The results confirmed that the presented structures have outperformed all prior designs and shows significant improvements in terms of power consumption, complexity, area occupation and input to output clock delay. We studied structures can lead to designing of more complex and high performance QCA nanoscale circuits. Correlation examination of successful zones utilized and control utilization ultra low power Quantum Dot Cell with scaled limit voltage decreases engendering deferral and power utilization with extensive sum. Impact of info vectors, postponement, power and supply variety.

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